2920-16
SIGNAL PROCESSOR

- **Real Time Digital Processing of Analog Signals**
- **Nominal Signal Bandwidths from DC to 10KHz**
- **Digital Processing Accuracy and Stability**
- **Special Purpose Instruction Set for Signal Processing**
- **INTELLEC® Compatible Development System Software and Hardware**
- **Multiple Analog Inputs and Outputs**
- **On-Chip Sample and Hold Circuits and D/A Converter**
- **On-Chip EPROM: User Programmable and UV Erasable**
- **On-Chip Scratch Pad Memory**
- **Analog and/or TTL Output Waveforms, User Selectable**
- **±5V Power Supplies**
- **N-MOS Process**
- **2920-16 (T_{CYC} = 600 nsec), 2920-18 (T_{CYC} = 800 nsec)**

The Intel® 2920 Signal Processor is a programmable, single chip analog and digital signal processor specifically designed to replace analog subsystems in real time processing applications. Its instruction set plus the high precision (25 bits) digital arithmetic logic unit provides the capability to implement very complex subsystems. Typical functions performed by the 2920 include: Lowpass and Bandpass filters with up to 20 complex pole and/or zero pairs; Threshold Detectors; Limiters; Rectifiers; up to 25-bit multiplication and division; approximations to nonlinear functions such as square law and logarithm; logical operations; Input and Output multiplexing of signals; logical outputs for decision type processing; and analog outputs for multifrequency oscillators, waveform generators, etc. In addition, several 2920's may be cascaded for very complex processing applications with no loss in throughput rate.

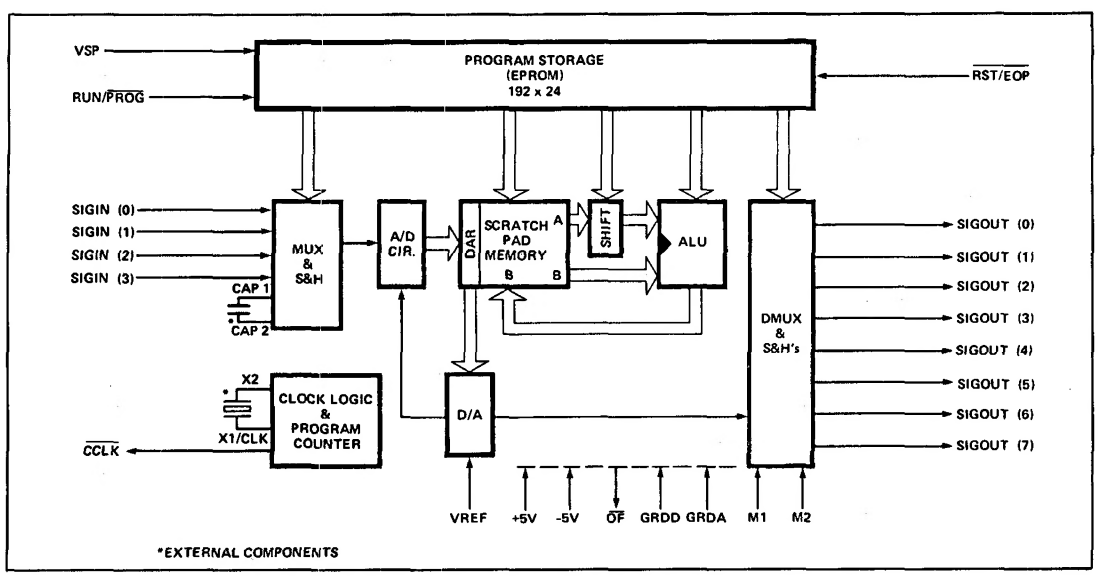


Figure 1. Functional Block Diagram (Run Mode).

PIN DESCRIPTIONS (RUN MODE)

Symbol	Function
SIGOUT	8 pins corresponding to the 8 demultiplexed analog outputs (0-7).
GRDA	Analog signal ground held at or near GRDD typically.
CAP_1 & CAP_2	External capacitor connections for the input signal sample and hold circuit.
VREF	Input Reference Voltage.
SIGIN	4 pins corresponding to the 4 multiplexed analog inputs (0-3).
V_{BB}	Most negative power pin set at −5 volts during run mode (different voltage in program mode).
X1/CLK	Clock input when using external clock signals, oscillator input for external crystal when using internal clock.
X_2	Oscillator input for external crystal when using internal clock.
GRDD	Digital ground.
V_{CC}	5 volts in run mode.
$\overline{CCLK}$	Internal fetch cycle clock output. The falling edge designates the START of a new PROM fetch cycle. $\overline{CCLK}$ is 1/16 of X1/CLK rate.
RUN/$\overline{PROG}$	Mode control tied to GRDD in run mode.
$\overline{RST}$/$\overline{EOP}$	Low $\overline{RST}$ input initializes program fetch counter to first location. As an output it signifies EOP instruction present (open drain, active low).
$\overline{OF}$	Indicates an overflow in the current ALU operation (open drain, active low).
VSP	EPROM power Pin 0 volts for RUN mode. (Different voltage in program mode.)
M1, M2	Two pins which specify the output mode of the SIGOUT pins (see Table 6).

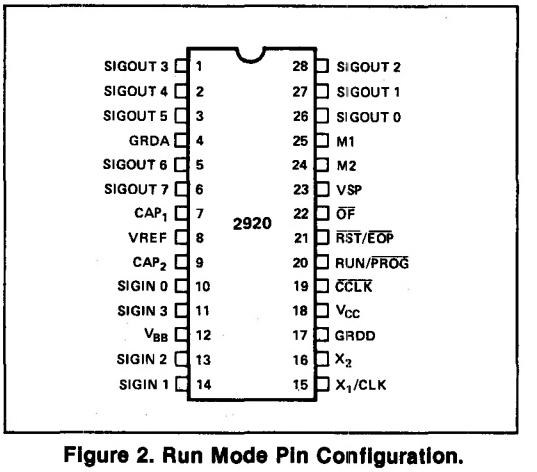


Figure 2. Run Mode Pin Configuration.

PIN DESCRIPTIONS (PROGRAM MODE)

Symbol	Function
D0,D1,D2,D3	4 pins carrying EPROM program data for both input and output (open drain, active low output; active high input).
V_{B1}, V_{B2}, V_{B3}	Digital ground in PROGRAM mode (different voltage for RUN mode).
V_{S1}, V_{S2}, V_{S3}	+5 volts in PROGRAM mode (function changes for RUN mode).
RUN/$\overline{PROG}$	Mode control pin tied to ground for PROGRAM mode (voltage changes for RUN mode).
$\overline{INCR}$	Input pulse increments the nibble (4-bits) counter in PROG mode (function changes in RUN mode).
VSP	EPROM power pin +5 volts for VERIFY mode and +25 volts for PROGRAM mode (different voltage in RUN mode).
PROG/$\overline{VER}$	Controls EPROM bi-directional data bus for verify (low) or program (high).
$\overline{RST}$	Input pulse resets nibble counter to position zero for start of programming.

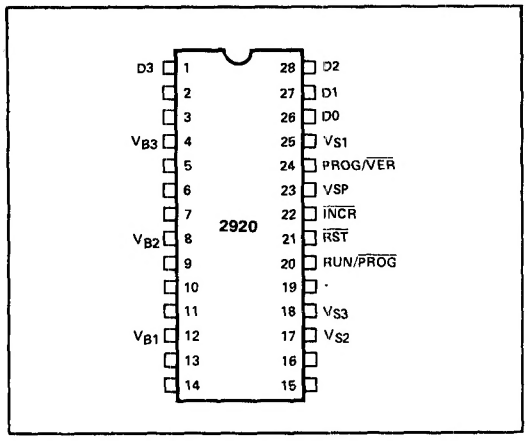


Figure 3. Program Mode Pin Configuration.

FUNCTIONAL DESCRIPTION

The Intel® 2920 is a programmable, single chip analog and digital signal processor which has been designed specifically to replace analog systems in real-time processing applications. The 2920 operates its analog circuitry simultaneously with the digital circuitry thereby achieving the efficiency and speed needed for real-time operation. Digital circuitry includes: EPROM program storage, RAM scratch pad memory, clock and timing circuitry, binary scaler, and the arithmetic logic unit (ALU). The analog circuitry is composed of 4 analog inputs, an input multiplexer, an input sample and hold (S&H), A/D and D/A converters, an output multiplexer, 8 analog outputs, and buffered output S&H's.

Once the EPROM is programmed, the 2920 is ready for operation as an analog subsystem. The following signal flow and operations can be described with reference to the functional block diagram shown in Figure 1.

Clock and Timing Logic — The 2920 can use an external clock or can generate its own clock with an external crystal placed across Pins 15 and 16. The program counter is incremented one instruction count for every 4 master clock cycles and continues to increment until it reaches a count of 191. Instructions are executed sequentially and no program jumps are provided. The sample rate is determined by the number of instructions in the program and the instruction cycle time. A 6.67 MHz clock (600 nsec instruction cycle time) and a full 192 instructions will result in a sample rate of 8,680 Hz.

Program Storage and Control — The EPROM is made up of 192 words with 24-bits per word. Each 24-bit word contains 6 instruction fields (see Table 1) which control the individual subsystems in the 2920.

RAM — The memory consists of a random-access read/write array organized as 40 words of 25-bits each. The address space is extended to provide constants and access to a register (DAR) for interfacing the memory-ALU with the analog conversion section. The RAM is a two port memory where the "A" location is Read Only and passes via a scaler to the ALU as one operand. The "B" location data passes to the ALU input as its second operand and the ALU result is written back to it. Both the RAM and the ALU represent data in two's complement format. All operations are performed in two's complement arithmetic. Program operations are simplified by assuming the binary point to the right of the sign bit.

An extended address space is used to generate constants within the program. It is accessed through the "A" port only and may be addressed using the last 16 locations of the "A" address field (i.e., "A" address 11XXXX). The constant is determined by the 4 least significant "A" address bits.

These 4 bits are treated as the 4 most significant bits at the input to the binary shifter. A sequence of extended addresses with shift operations can generate any constant up to 25 bits long.

The DAR is 9 bits wide and can be accessed in several ways. As a memory location, the DAR occupies the 9 most significant bit positions of the 25-bit word and can be accessed as "A" and/or "B" port. The DAR output is also tied directly to the D/A converter inputs and is used as a successive approximation register for A/D conversion under control of the analog function instruction fields. Each bit position of the DAR can also be selected and tested for conditional arithmetic operations.

Binary Shifter — The 2920 has a binary shifter between the memory "A" port output and the ALU "A" operand input. This feature allows the "A" operand to be scaled by any magnitude between 2^2 and 2^{-13} (left shift 2 to right shift 13). When a number is shifted right vacated bit positions are filled with the sign bit. (2's complement arithmetic shift). Shift op codes are shown in Table 2.

ALU — The Arithmetic-Logic Unit calculates a 25-bit result based on an operation performed on the scaled "A" and the "B" operands delivered from memory. The 25-bit result is written back into the "B" memory location near the end of the instruction cycle. The ALU has logic to accommodate the left shift scaling. For arithmetic operations, this logic is used to calculate a 25-bit result for normal operations and to maintain the sign bit

when an overflow occurs. An overflow occurs only when the magnitude of the result is larger than the largest number that can be stored in memory (25 bits). In that event, the result is set to the largest magnitude value with the correct sign. This overflow algorithm protects the continuity of the digitized analog signals and helps maintain the stability of the signal processing functions implemented. It is analogous to an overdriven amplifier going into saturation.

Instruction Set — The 2920 assembler uses the following program format to specify the 24-bit instruction word stored in the EPROM:

All processing subsystems are implemented using a combination of analog and digital instructions to input and output signals and/or data, and to realize the processing functions respectively.

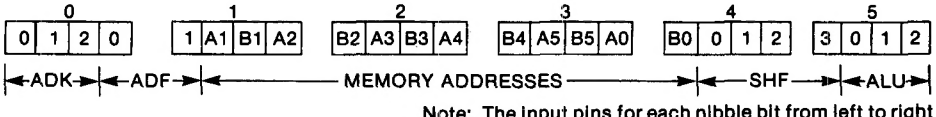
The analog input and output instructions are IN(K) and OUT(K) respectively. A sequence of IN(K) instructions followed by the sign conversion and amplitude conversion instructions CVTS and CVT(K) respectively are used to perform the input A/D conversion. A simple sequence of OUT(K) instructions is all that is needed to output a 9-bit amplitude on channel K. Other analog instructions are the EOP instruction which must be placed at ROM location 188, NOP which is simply a no-operation, and CNDS or CND(K) which are conditional operators which select and test a bit in the DAR for the conditional ADD or LDA instructions or define the destination of the carry bit for the conditional SUB instruction.

The ALU arithmetic instructions are ADD,SUB,LDA which perform the operations of addition, subtraction, and data transfer respectively. When these instructions are conditioned, they may be used to perform multiplication or division by a variable or data dependent switching.

Other digital instructions include the absolute value ABS, the absolute value and add ABA, and the ideal limit instruction LIM.

These instructions and their corresponding op codes are detailed in Table 3.

Table 1. Nibble Organization For Loading Program



Note: The input pins for each nibble bit from left to right are D0, D1, D2, D3.

Table 2. Shift OP Codes

Operation	Mnemonic	Op Code				Scale Factor
		3	2	1	0	
Shift Right 13 Bits	R13	1	1	0	0	2^{-13}
Shift Right 12 Bits	R12	1	0	1	1	2^{-12}
⋮	⋮	⋮	⋮	⋮	⋮	⋮
Shift Right 1 Bit	R01	0	0	0	0	2^{-1}
No Shift	R00	1	1	1	1	1
Shift Left 1 Bit	L01	1	1	1	0	2
Shift Left 2 Bits	L02	1	1	0	1	4

Table 3. Instruction Set And OP Codes

Mnemonics		Op-Codes[1]			Operations			Notes
Code	Condition	ALU	ADF	ADK				
Digital Instructions		0,1,2	0,1	2,1,0				
ADD		011	↑	↑	$(Ax2^N) + B \longrightarrow B$			
SUB		101			$B - (Ax2^N) \longrightarrow B$			
LDA		111			$(Ax2^N) + 0 \longrightarrow B$			
XOR		000			$(Ax2^N) \oplus B \longrightarrow B$			
AND		100			$(Ax2^N) \cdot B \longrightarrow B$			
ABS		110			$\lvert(Ax2^N)\rvert \longrightarrow B$			
ABA[11]		001	[3]	[3]	$\lvert(Ax2^N)\rvert + B \longrightarrow B$			
LIM		010			$Sign(A) \rightarrow \pm$ F.S. $\rightarrow B$[4]			
ADD	CND( )[2]	011			$(Ax2^N) + B \longrightarrow B$	IFF DAR(K) = 1		
					$B \longrightarrow B$	IFF DAR(K) = 0		
SUB	CND( )[2][8]	101			$B - (Ax2^N) \longrightarrow B$	& CY → DAR(K)	IFF $CY_P = 1$	[5]
					$B + (Ax2^N) \longrightarrow B$	& CY → DAR(K)	IFF $CY_P = 0$	
LDA	CND( )[2]	111			$(Ax2^N) \longrightarrow B$	IFF DAR(K) = 1		
					$B \longrightarrow B$	IFF DAR(K) = 0		
ABA[11]	CND( )[9]	001			$(Ax2^N) + B \longrightarrow B$			
XOR	CND( )[9]	000			$(Ax2^N) \oplus B \longrightarrow B$			
Analog Instructions								
IN(K)		↑	00	0-3	Signal Sample from Input Channel K			
OUT(K)			10	0-7	D/A to Output Channel K			
CVTS			00	6	Determine Sign Bit			
CVT(K)			01	0-7	Perform A/D on Bit K			
EOP		[7]	00	5	Program Counter to Zero			[6]
NOP			00	4	No Operation			
CND(K)			11	0-7	Select Bit K for Conditional Instructions			
CNDS		↓	00	7	Select Sign Bit for Conditional Instructions			

Notes:
1. Op codes ALU and ADF are in binary notation, ADK is in decimal notation and represents the value "K" when appropriate.
2. CND( ) can be either CND(K) or CNDS testing amplitude bits or the sign bit of the DAR respectively.
3. Determined by analog instructions below.
4. B is set to full scale (F.S.) amplitude with the same sign as the "A" port operand.
5. The previous carry bit (CY_P) is tested to determine the operation. The present carry bit (CY) is loaded into the Kth bit location of the DAR. "Present carry (CY) is generated independent of overflow. It will represent the carry (CY) of a calculated 28-bit result."
6. EOP will also enable overflow correction if it was disabled during a program pass. The EOP must occur in ROM location 188.
7. Determined by digital instructions above.
8. For SUB CNDS operation CY ← DAR(S).
9. Does not affect DAR. In this case, CND is used with XOR/ABA to enable/disable the ALU overflow saturation algorithm. Use of either instruction causes the ALU output to roll over rather than go to full scale with sign bit preserved. An EOP instruction will also enable the ALU overflow saturation algorithm.
10. Clarification of CY_{OUT} sense for certain operations. For LDA, XOR, AND, ABS; $CY_{OUT} \rightarrow 0$.
11. Recommend that the ABS & ADD instructions be used in place of ABA. The ABA instruction typically runs 2 MHz slower. The saturation logic, however can be set and reset at full speed.

Input Multiplexer and S&H — The input channels consist of four analog sampling switches which use a common external sampling capacitor. The external capacitor should be approximately 500pF to yield an offset of less than −½ LSB. The acquisition time should be approximately six times the RC time constant of the sample and hold circuitry (i.e. 500 pF times 1.5KΩ equals 750 nsec.). Acquisition time equal to six or more time constants should keep the input crosstalk to below -54dB. For systems which require less dynamic range, the input acquisition time can be reduced. For a 600 nsec. cycle approximately eight IN(K) instructions would be required. For serial digital inputs, fewer IN(K) instructions can be used. For systems with 2920 cycle times much greater than 600 nsec., the external sampling capacitor should be increased to 1000 pF to reduce the droop rate with a corresponding increase in the RC time constant.

A/D-D/A Conversion — The successive approximation analog to digital conversion is performed under program control. It uses the CVTS instruction first to set the sign bit and the CVT(K) instruction to determine the value of the Kth DAR bit starting with the MSB. NOPs equivalent to 1.2 usec. must follow each CVT(K) instruction to allow the D/A to settle. All A/D conversions of 2 bits or more must have "ADD DAR, KM2, RO, CND6" immediately following the CVTS instruction followed by NOPs equivalent to 1.2 usec. In addition, after CVT3, CVT2, and CVT1, "LDA X,X,RO,CND4" must immediately follow the CVT instruction with additional time in NOPs to meet the 1.2 usec. minimum before the next CVT(K) instruction. The CND4 instructions are required to minimize input crosstalk. The suggested conversion sequence for nine bit resolution with the 2920 cycle time equal to 600 nsec. is shown below in Table 4. Digital inputs and inputs with less than nine bits resolution will have a shorter sequence.

Table 4. Suggested Input And Conversion Sequence

Digital	Analog	Digital	Analog
. . . .	IN(K)	. . . .	CVT5
. . . .	IN(K)	. . . .	NOP
. . . .	IN(K)	. . . .	NOP
. . . .	IN(K)	. . . .	CVT4
. . . .	IN(K)	. . . .	NOP
. . . .	IN(K)	. . . .	NOP
. . . .	IN(K)	. . . .	CVT3
. . . .	IN(K)	LDA X,X,R0,	CND4
. . . .	NOP	. . . .	NOP
. . . .	CVTS	. . . .	CVT2
ADD DAR,KM2,RO,	CND6	LDA X,X,R0,	GND4
. . . .	NOP	. . . .	NOP
. . . .	NOP	. . . .	CVT1
. . . .	CVT7	LDA X,X,RU,	CND4
. . . .	NOP	. . . .	NOP
. . . .	NOP	. . . .	CVTO
. . . .	CVT6		
. . . .	NOP		
. . . .	NOP		

Continue Next Column

where "•" equals available digital instruction

Output Demultiplexer and S&Hs — The 2920's eight analog output channels include a sample and hold circuit per channel demultiplexed from a common, buffered D/A output. Two rules for outputting samples are: (1) No outputting should be done while writing to the DAR. (2) A sequence of analog NOP instructions equal to 6 usec. should be used to settle the D/A converter, and a sequence of OUT(K) instructions equal to 1 usec. should be used to settle the S&H output. In addition, to minimize output crosstalk, a dummy output to an unused channel should be performed prior to outputting to the desired channel. The suggested sequence for a nine bit resolution output with a 600 nsec. cycle time is outlined in Table 5. For outputs that require less than nine bits resolution or digital outputs, the number of NOPs and OUT(K)s can be reduced.

Table 5. Suggested Output Sequence

DIGITAL	ANALOG
LDA,DAR,X,R0,	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	NOP
. . . . .	CND(X)
. . . . .	OUT(X)
. . . . .	OUT(X)
. . . . .	OUT(K)
. . . . .	OUT(K)

where K = desired output and X = wasted output
K ≠ X, "•" available digital instruction.

Conditional operations should not immediately precede or follow an OUT instruction. Otherwise a CND(K) may affect the value of the Kth output.

TTL Output — The SIGOUT(K) pins can be selected to be either analog out or TTL compatible as seen in Table 6. The analog mode allows the full 9-bit D/A output to be present. The TTL mode requires a L/M instruction to yield a "0" or "1" decision. This output can be presented to the SIGOUT(K) pins and is compatible to a single TTL gate or equivalent. The internal threshold required is ± 1.5 volts for a high level output. An external pullup resistor to V_{CC} is also required.

Table 6. Output Mode For Sigout Pins As Function Of M1 And M2

M1	M2	SIGOUT Pins
5V	5V	0-7 Analog
5V	-5V	0-3 Analog, 4-7 TTL
-5V	5V	0-3 TTL, 4-7 Analog
-5V	-5V	0-7 TTL

Reference Voltage — The internal D/A converter requires a single positive reference voltage (VREF) to establish its voltage range. This user supplied reference can range from 1V to 2V. The

resulting input and output signal voltage range is ± VREF. For full 9-bit resolution and best linearity, VREF = 1V. If the TTL output is required, VREF > 1.5V is necessary. The minimum voltage step (LSB) of the D/A converter is $V_{REF}/256$ volts. Voltage variations on V_{REF} will appear as noise to the D/A converter. It is therefore necessary to provide a noise free voltage source for the reference. The input signal voltage range is (± VREF) – ½ LSB. Recommended maximum negative output is – 1.0 volts.

2920 DEVELOPMENT SUPPORT TOOLS

Support tools for the 2920 are based on the Intellec® Microcomputer Development Systems. A 2920 Software Support Package (SPS-20) consisting of the Signal Processing Applications Software/Compiler (SPAS-20), the 2920 Software Simulator, and the 2920 Assembler is available to facilitate design and development efforts. EPROM programming support includes the Intel EPROM programmer and the 2920 personality module (UPP-820). A complete Signal Processing Support System (MCI-20-DS1) consisting of the Microcomputer Development System, the 2920 Software Support Package, the EPROM programmer and personality module is recommended and is available at a reduced price.

The 2920 Signal Processing Applications Software/Compiler is an interactive tool for designing software to be executed on the 2920 Signal Processor. The compiler accepts English-like statements from the user and generates 2920 assembly language code.

The assembler translates symbolic 2920 assembly language programs into the machine operation codes. The user can load the codes into the 2920 simulator or to the Universal EPROM Programmer for programming the 2920 itself.

The simulator, operating entirely in software, allows the user to test and debug 2920 programs. The user can specify input signals, simulate program execution, set-up breakpoints, display input and output, display and alter the contents of the 2920 registers and memory locations, and to graph the output waveforms.

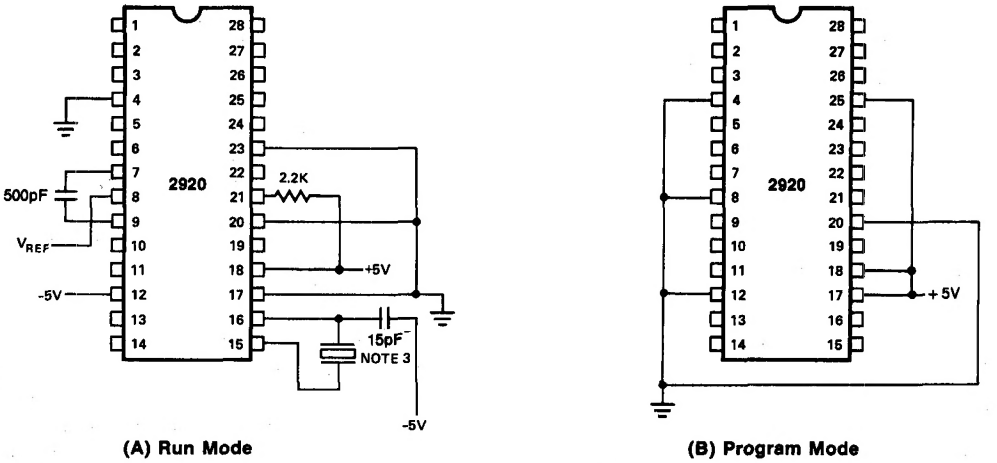
The compiler, assembler and simulator enable the designer to develop and test an entire program without programming the device. The 2920 designer works at the Intellec® Microcomputer Development System rather than at a breadboard. The development system facilitates the designing and testing of 2920 applications.

EPROM PROGRAMMING

The 2920 EPROM in the programming mode is arranged as a 1152 by 4-bit memory. Each instruction (24-bits) is loaded as 6 nibbles (4-bits) as seen in Table 3. Figure 7 shows the timing relationships of the signals required to program and verify the EPROM contents. In the program mode all voltages are referenced to V_{BB} which is set to digital ground, thereby allowing TTL logic to be used for controlling the programming cycle. The D pins are bidirectional with the direction controlled by the PROG/$\overline{\text{VER}}$ pin. A high level at the PROG/$\overline{\text{VER}}$ pin switches to input mode, a low to output mode (see Figure 7). This feature allows the programmed data to be verified before going on to the next address.

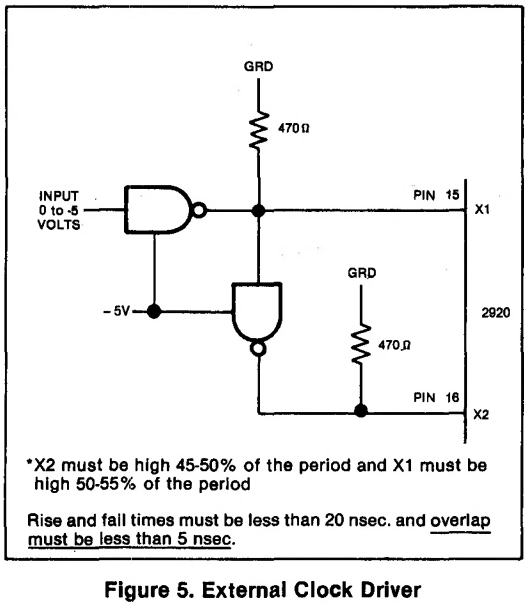
The internal nibble counter is incremented during the falling edge of $\overline{\text{INCR}}$. 1152 INCR transitions will complete the full program cycle. To initialize at address (nibble) 0, RST must be pulsed low, then $\overline{\text{INCR}}$ can be issued. From then on, programming is accomplished according to Figure 7.

The RUN/$\overline{\text{PROG}}$ pin must be tied to V_{BB} and VSP should be pulsed between ± 5V and + 25 ± 1V at 15mA maximum. The D pins have an open drain in the output direction.



Notes:
1. Analog grounding is connected to the GRDA lead. The GRDA and GRDD lead are not connected inside the 2920. An external connection is thus necessary outside the device to tie all the analog ground lines to the common return of the system GRDD. That external connection has to have a minimal impedance (ground plane) to avoid a DC offset in the 2920.
2. Pullup resistor at Pin 21 is only required if an EOP instruction is used.
3. Stray capacitance must also be considered. The sum should not exceed 15pF.
4. Opaque tape must cover EPROM window during run mode.

Figure 4. Typical Power Hookups for Run and Program Mode



*X2 must be high 45-50% of the period and X1 must be high 50-55% of the period

Rise and fall times must be less than 20 nsec. and overlap must be less than 5 nsec.

Figure 5. External Clock Driver

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −40°C to ±80°C
Storage Temperature . . . . . −65°C to ±150°C
Supply Voltage with Respect to V_{BB} . . . . −0.5V to ±14V
All Input Voltages . . . . . −0.5V to (V_{CC} ±1V)
Outputs . . . . . −1V to (V_{CC} ±1V)
Power Dissipation 1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS (Run Mode)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

ANALOG (SIGIN(K), SIGOUT(K))

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
Z_I	Input Impedance		100		KΩ	Unsampled input
Z_{SH}	S&H Impendance		1.5		KΩ	Series resistance with S&H
	A/D Resolution			9	bits	
	Input Differential Linearity		±1		LSB	
	Input Integral Linearity		±1		LSB	
T_A	Aperture		5		nsec	Equivalent SNR = 60dB @ 10KHz
X_I	Input Crosstalk		−54		dB	Input to input*
V_{ID}	Input Droop Rate		50		uv/us	500pF cap. with dark cover
V_{IR}	Input Voltage Range			±VREF	V	
V_{IOS}	Input Zero Offset		8		mV	
I_{IZC}	Input Zero Crossing Error		12		mV	
G_I	Input Gain		1			
	Gain Error		2		%	ratio of Neg. & Pos. gains
T_{IA}	Input Acquistion Time		4,500		nsec	9 bit resolution*
Z_O	Output Impedance		1		KΩ	
I_O	Output Drive Current		400		μA	20pF load
	D/A Resolution			9	bits	
	Output Differential Linearity			±½	LSB	SIGOUT load 100KΩ −1 < SIGOUT < 1
	Output Integral Linearity		±1		LSB	SIGOUT load 100K −1 < SIGOUT < 1
X_O	Output Crosstalk		−54		dB	Output to output*
V_{OD}	Output Droop Rate		0.2		mv/us	@ 70°C with dark cover
V_{OR}	Output Voltage Range	−1.0		+1	V	
V_{OOS}	Output Zero Offset			−100	mV	
V_{OZC}	Output Zero Crossing Error		8		mV	
G_O	Output Gain	0.85			V/V	
	Gain Error			15	%	ratio of Neg. & Pos. Gains
T_{OA}	Output Acquistion Time		6,000		nsec	9 bit resolution*
G_T	Throughput Gain		.85		V/V	A/D to D/A
VREF	Voltage Reference Level	1.0		2.0	V	
I_{VR}	Voltage Reference Current	60		115	μA	VREF equal 1 volts

DIGITAL ($\overline{OF}$, $\overline{CCLK}$, $\overline{EOP}$ in TTL Mode)

I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} < V_{IH}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{IXL}	Input Low Voltage, XI/CLK	−4.5		−5	V	
V_{IXH}	Input High Voltage, XI/CLK	−1		0	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2.5mA$, CCLK ONLY

*See text for explanation

POWER DISSIPATION

Symbol	Parameter	Limits Min.	Typ.	Max.	Units	Test Conditions
I_{CC}	Operating Current		30	50	mA	$V_{CC}=5V \pm 5\%$
I_{BB}	Operating Current		110	150	mA	$V_{BB}=5V \pm 5\%$

A.C. CHARACTERISTICS (Run Mode)

$T_A=0°C$ to $+70°C$, $V_{CC}=5V$, $V_{BB}=-5V$

F_{OSC}		4.0		6.67	MHz	Oscilator frequency
T_{CYC}	Instruction Cycle Period 2920-16	600			ns	4 clock cycles
	2920-18	800			ns	
T_{CE}	Cycle Start to EOP Valid		100		ns	
T_{EH}	EOP Hold Time		$T_{CYC}/8$		μs	
T_{FH}	OF Release Time		$T_{CYC}/8$		ns	
T_{CW}	CCLK Pulse Width		T_{CYC}		ns	Equals T_{CYC}

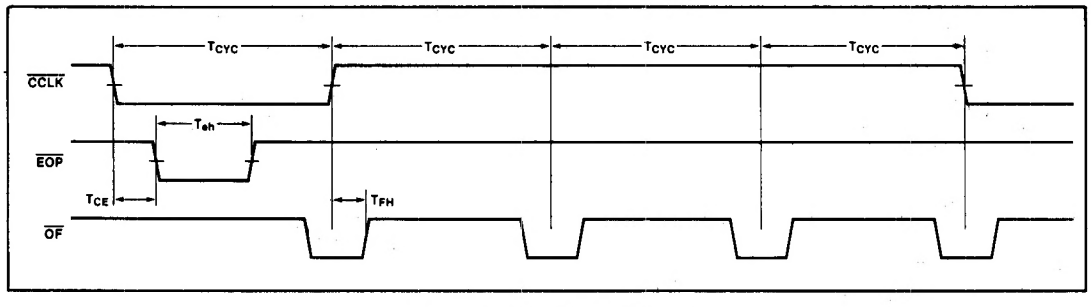


Figure 6. Run Mode Timing.

D.C. AND OPERATING CHARACTERISTICS (Program Mode)

T_A = 0°C to +70°C, V_{SS} = 5V, V_{BB} = 0V

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{TL}	Low Level Input Current			10	μA	$V_{IN}<V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN}>V_{IH}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.8	V	I_{OL} = 2.5mA
I_{SP}	Program Pulse Current			16	mA	Data Input = 0000
V_{P1}	Program Pulse ON Voltage	24	25	26	V	
V_{P2}	Program Pulse OFF Voltage		5		V	

POWER DISSIPATION (Program Mode)

I_{SS}	Operating Current		100		mA	V_{SS} = 5V + 10%

A.C. CHARACTERISTICS (Program Mode) $T_A = 0°C$ to $+70°C$, $V_{SS} = 5V$, $V_{BB} = 0V$

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
T_{RW}	Reset Pulse Width	1000			ns	
T_{RS}	Reset to Increment Set-Up	200			ns	
T_{RH}	Reset Hold	300			ns	
T_{IW}	Increment Pulse Width	1			μs	
T_{VP}	Data In Set-Up to Prog. Pulse	2			μs	
T_{PW}	Program Pulse Width	50		55	ms	
T_{PVI1}	Program to Verify Settling	1			μs	
T_{ACC}	Verify Access Time	20			μs	
T_{VI}	End of Verify to Increment	100			ns	

Note: 1. VSP must not undershoot 5V by more than 0.5V. Add undershoot settling time to T_{PV}.

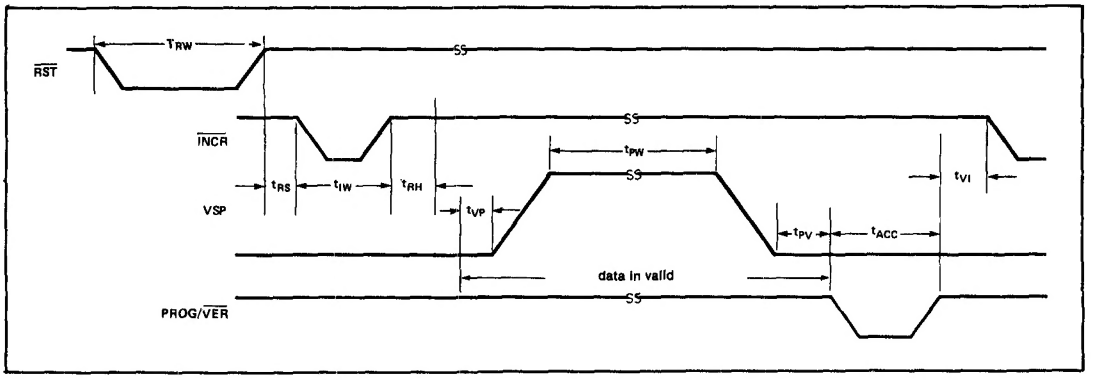


Figure 7. Program Mode Timing.